ModelSim XE III Tutorial

This is a brief tutorial on how to run the ModelSim VHDL editor and the ModelSim waveform generator.

Creating a place to save your work

First in "My Documents" create a folder named "ES4"
Within this folder create one called "Labs"

Setting Up ModelSim

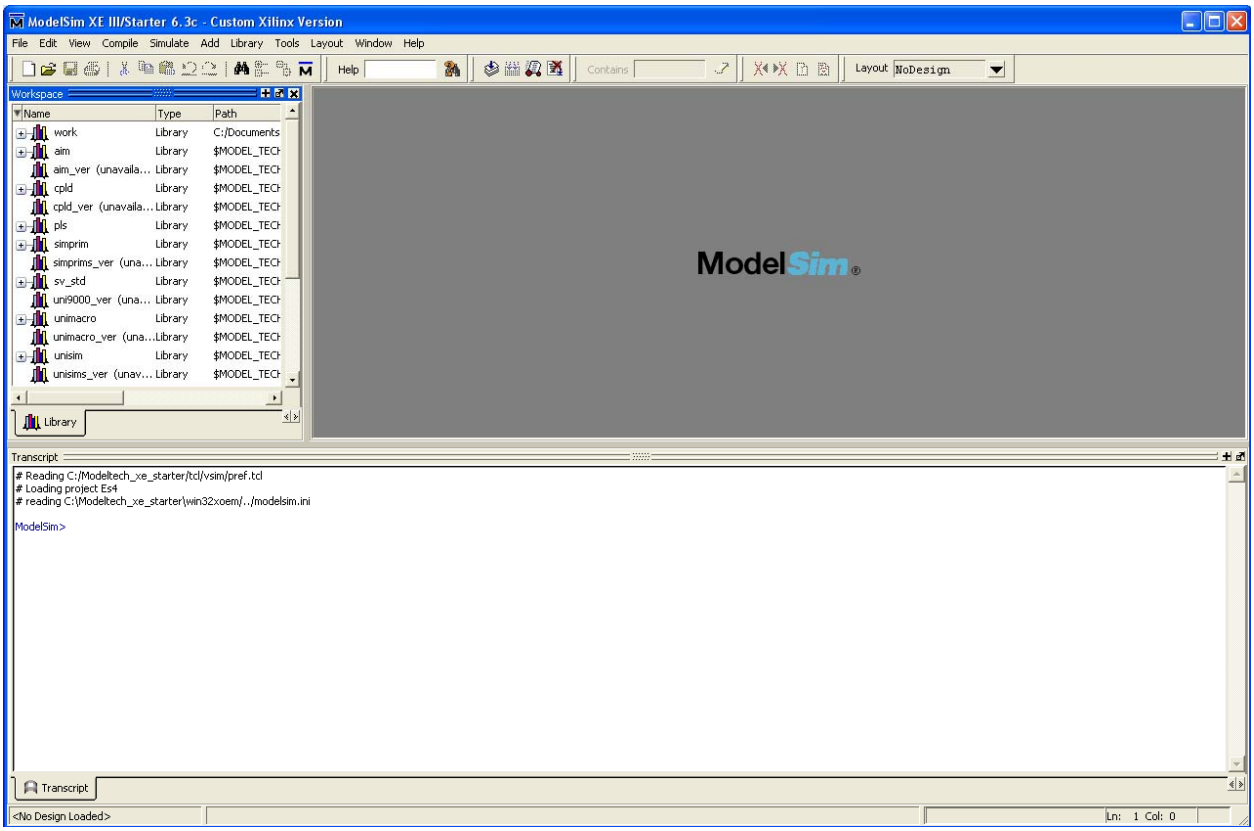
Before starting, check to see if ModelSim has been registered.
Click "Start" to "All Programs" to "ModelSim XE III 6.0a" to "ModelSim"
If the program starts up, then no registration is needed.
If the ModelSim flashes but the program does not start, then then ModelSim needs to be registerd.

Regsitering ModelSim

Click "Start" to "All Programs" to "ModelSim XE III 6.0a" to "Licensing Wizard"
Click "Continue"
On the following screen, click "Browse" and navigate to or type in
“C:\Modeltech_xe_starter\license.dat” or “C:\Modeltech_xe_starter\win32xoem\license.dat"
Click Continue and let the program register itself

Now start the ModelSim Project Navigator

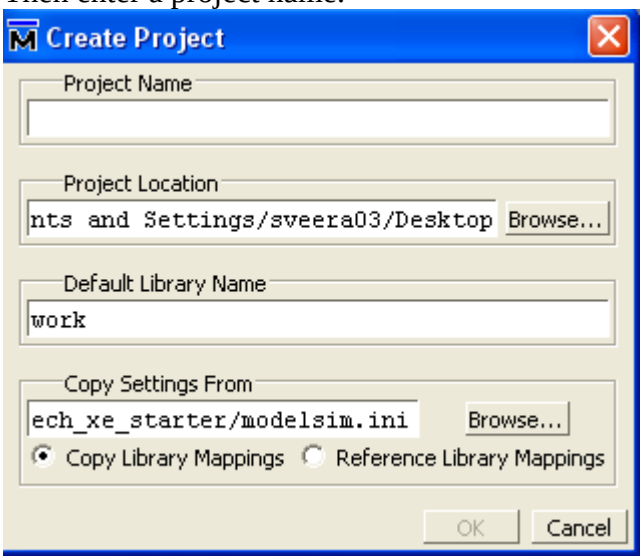
Click "Start" to "All Programs" to "ModelSim" to "Project Navigator"
You should get a screen similiar to the following



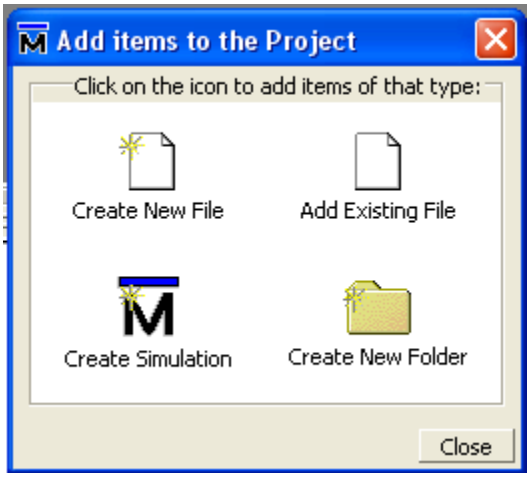
Creating a Project

Click on "File" and then "New Project"
In the "Project Location:" point it ot where your folder has been created

Then enter a project name.



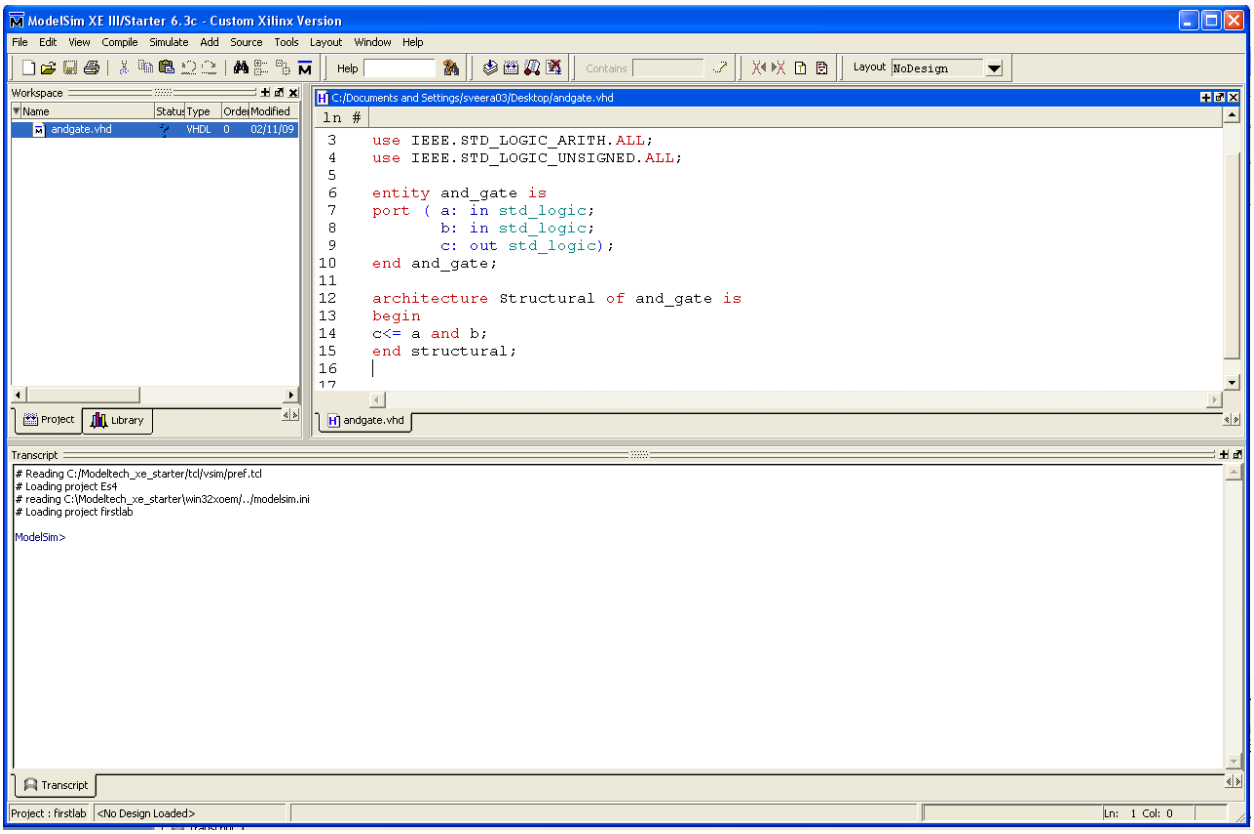
Click "OK" and select “Create a New File” from the pop-up menu.



Type the file name for example “andgate” and select the file type as VHDL. This will create a file name andgate.vhdl which is visible in the work space window.

Editing VHDL

Now, double click on the link ‘andgate.vhdl” in the work space window to invoke the vhdl editor that you can type in your program.



Enter in the VHDL code between the "begin" and "end" of the structural and the and gate will be done

and_gate.vhd

```
1  library IEEE;
2  use IEEE.STD_LOGIC_1164.ALL;
3  use IEEE.STD_LOGIC_ARITH.ALL;
4  use IEEE.STD_LOGIC_UNSIGNED.ALL;
5
6  --  Uncomment the following lines to use the declarations that are
7  --  provided for instantiating Xilinx primitive components.
8  --library UNISIM;
9  --use UNISIM.VComponents.all;
10
11 entity and_gate is
12     Port ( a : in std_logic;
13            b : in std_logic;
14            c : out std_logic);
15 end and_gate;
16
17 architecture Structural of and_gate is
18
19 begin
20      c <= a and b;
21 end Structural;
22
```

After editing the code, save the file (Ctrl+S)

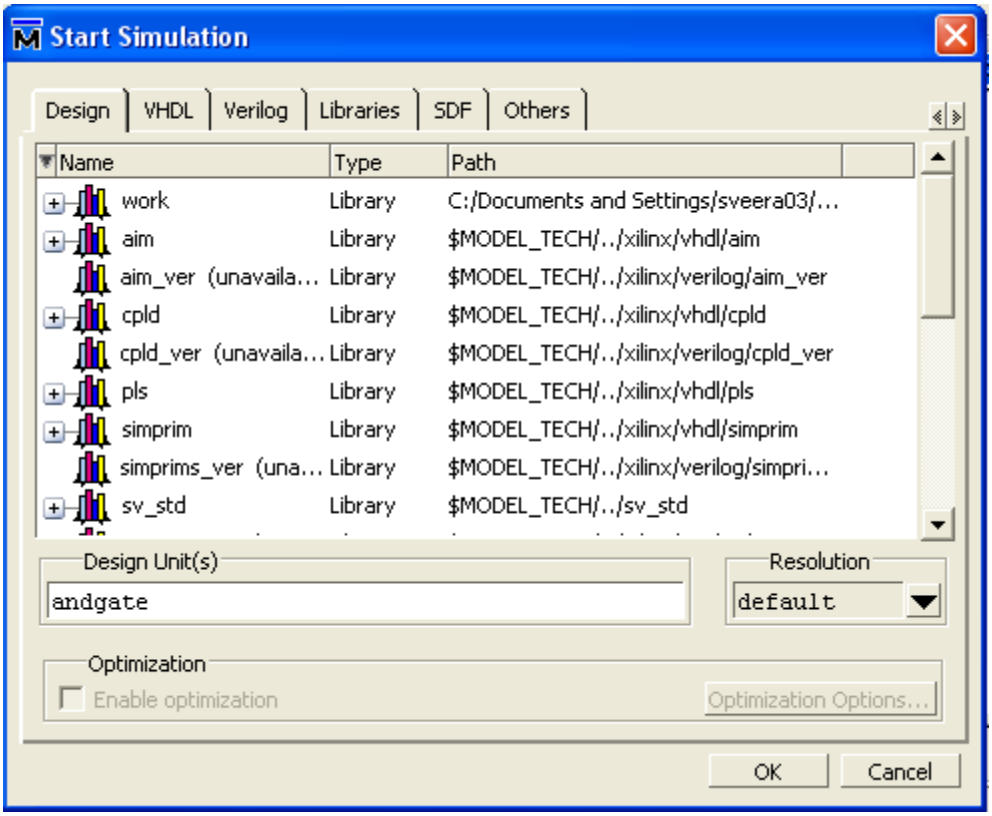
Compilation

Click on Compile in the Tool bar and select Compile All. The message appearing should say

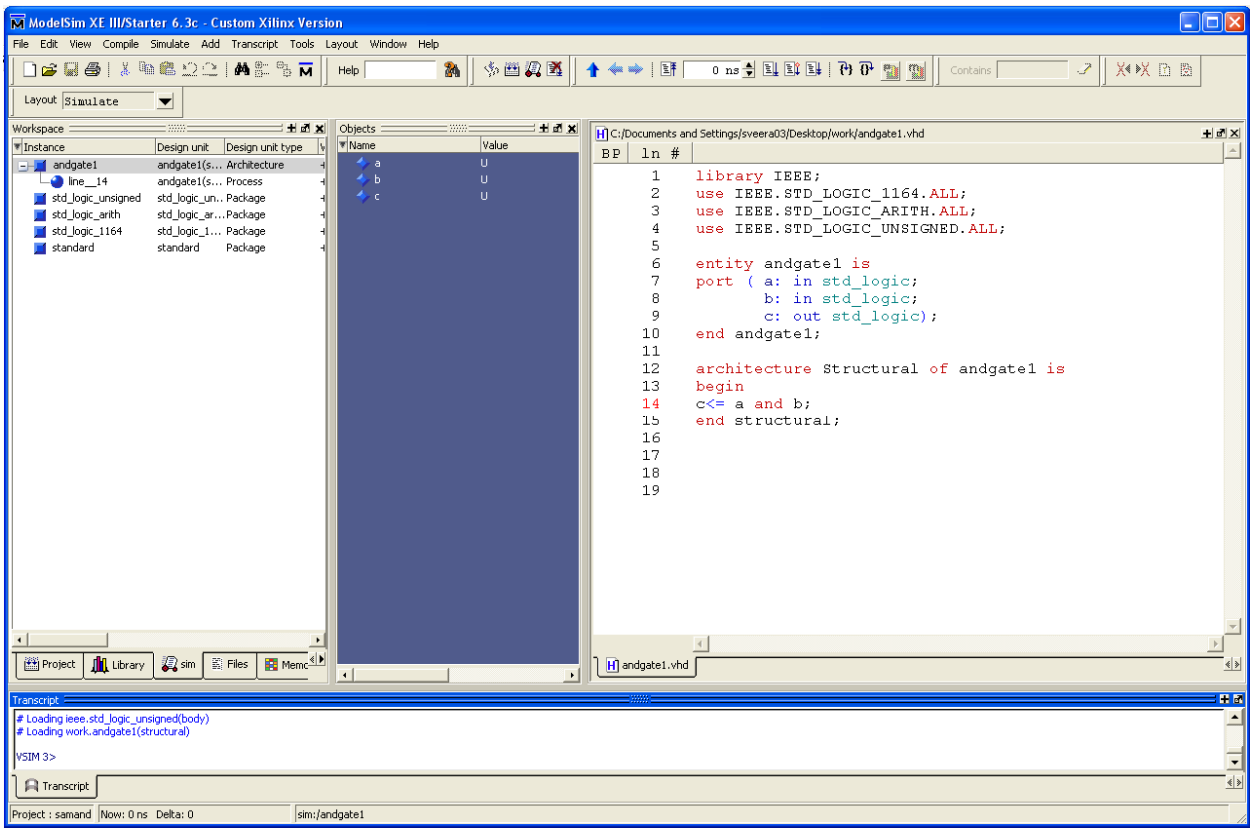
Compile of andgate.vhd was successful.

Simulation

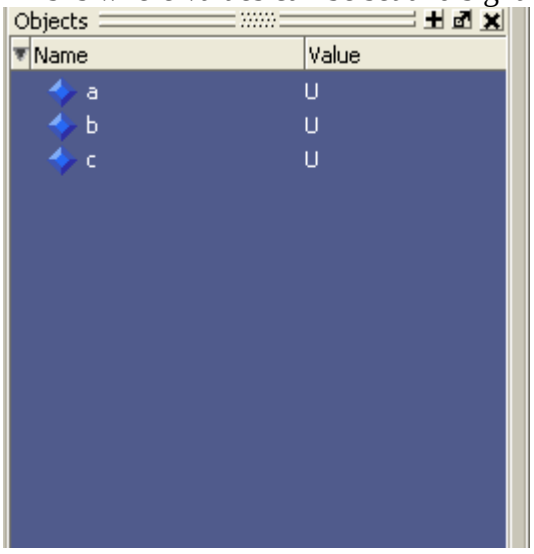
To start the simulation click on the Simulation menu from the Tool bar and select “Start Simulation”. And enter the name of the entity from your code in the pop-up menu, in this case “andgate”.



The next window should appear

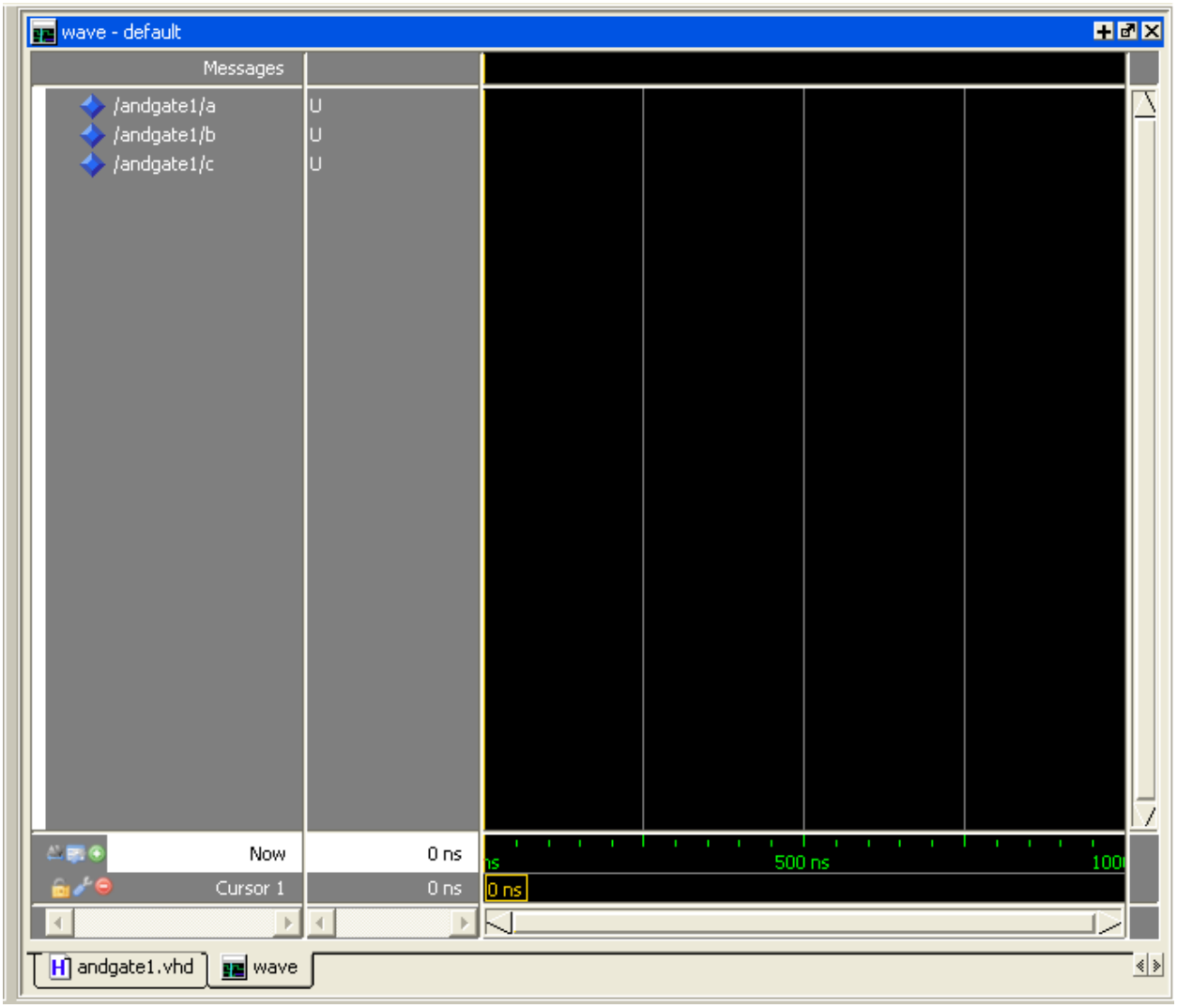


The Objects window will display the signals available
This is where values can be set and signals can be added to the waveform



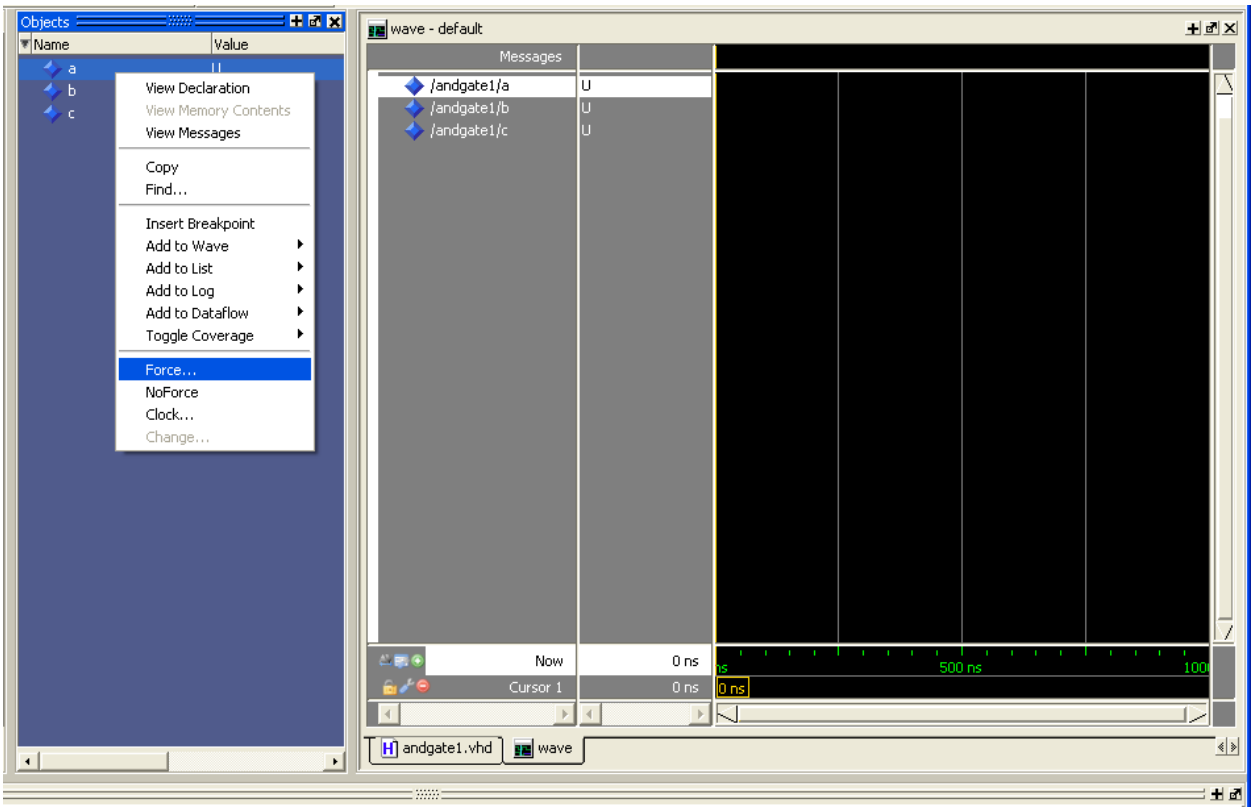
To add a signal, select the signal, right click on the signal "Add to Wave" then "Selected Signals"

The Wave window will be where your data will output to

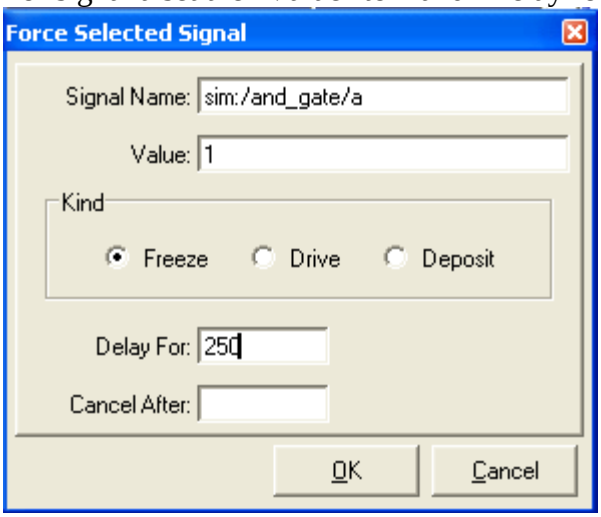


Editing in ModelSim

To test the and gate, several parameters will need to be set
Select a waveform, and click "Edit" to "Force"

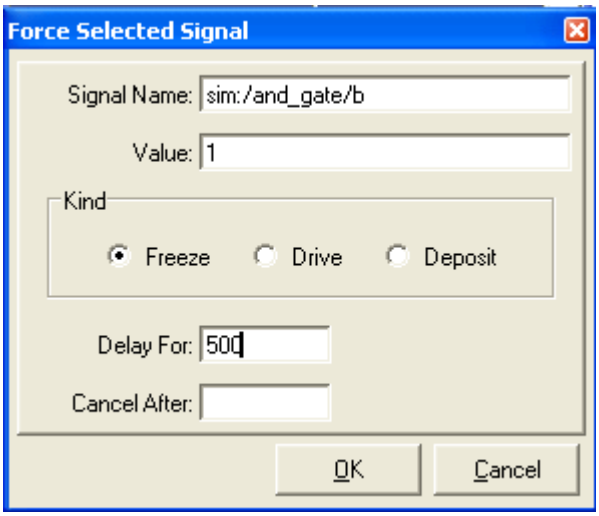


For signal a set the "Value" to 1 and "Delay for" to 250



This will set the value of a to be 1 after 250ps

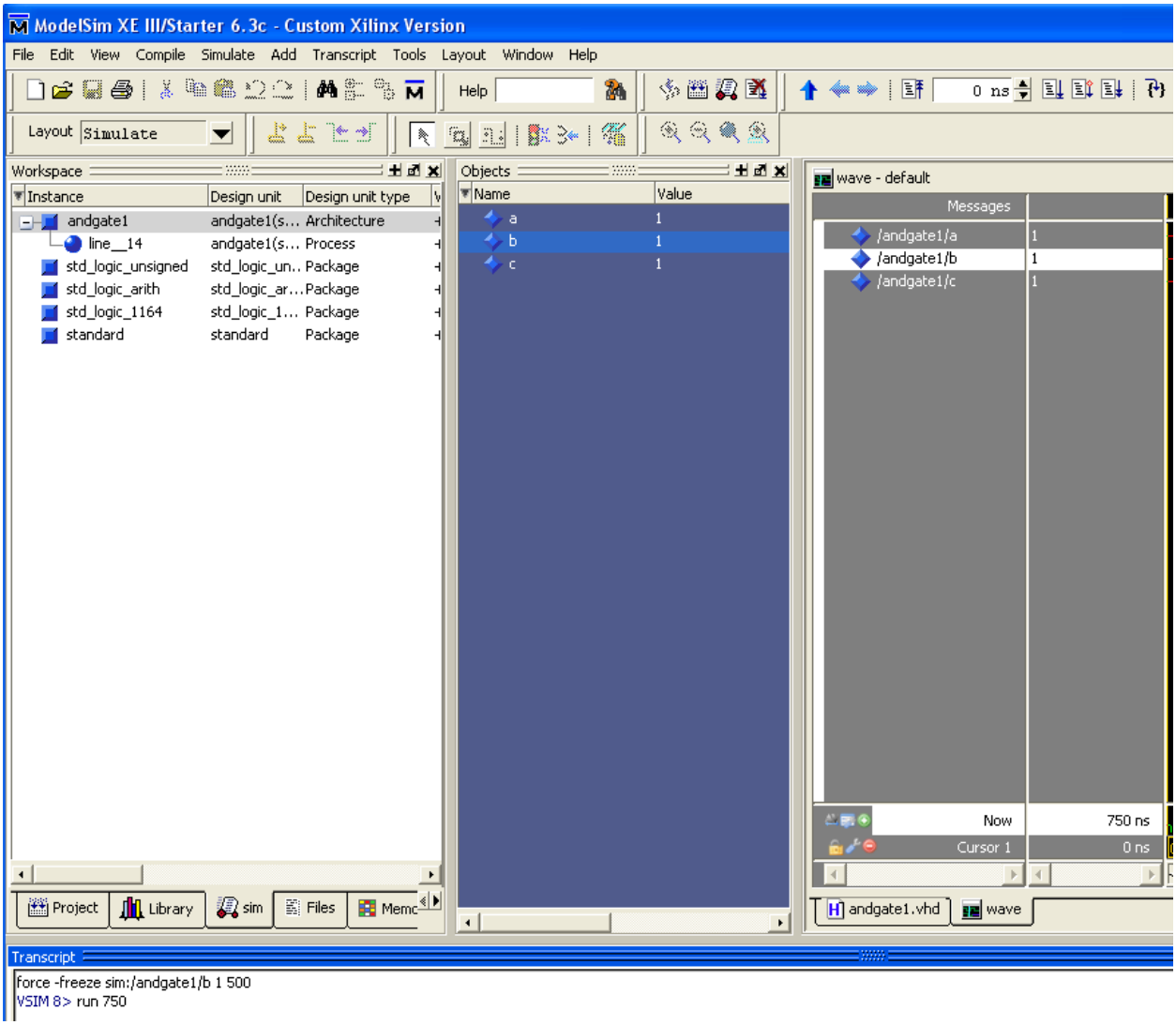
For signal b set the "Value" to 1 and "Delay for" to 500



This will set the value of a to be 1 after 250ps

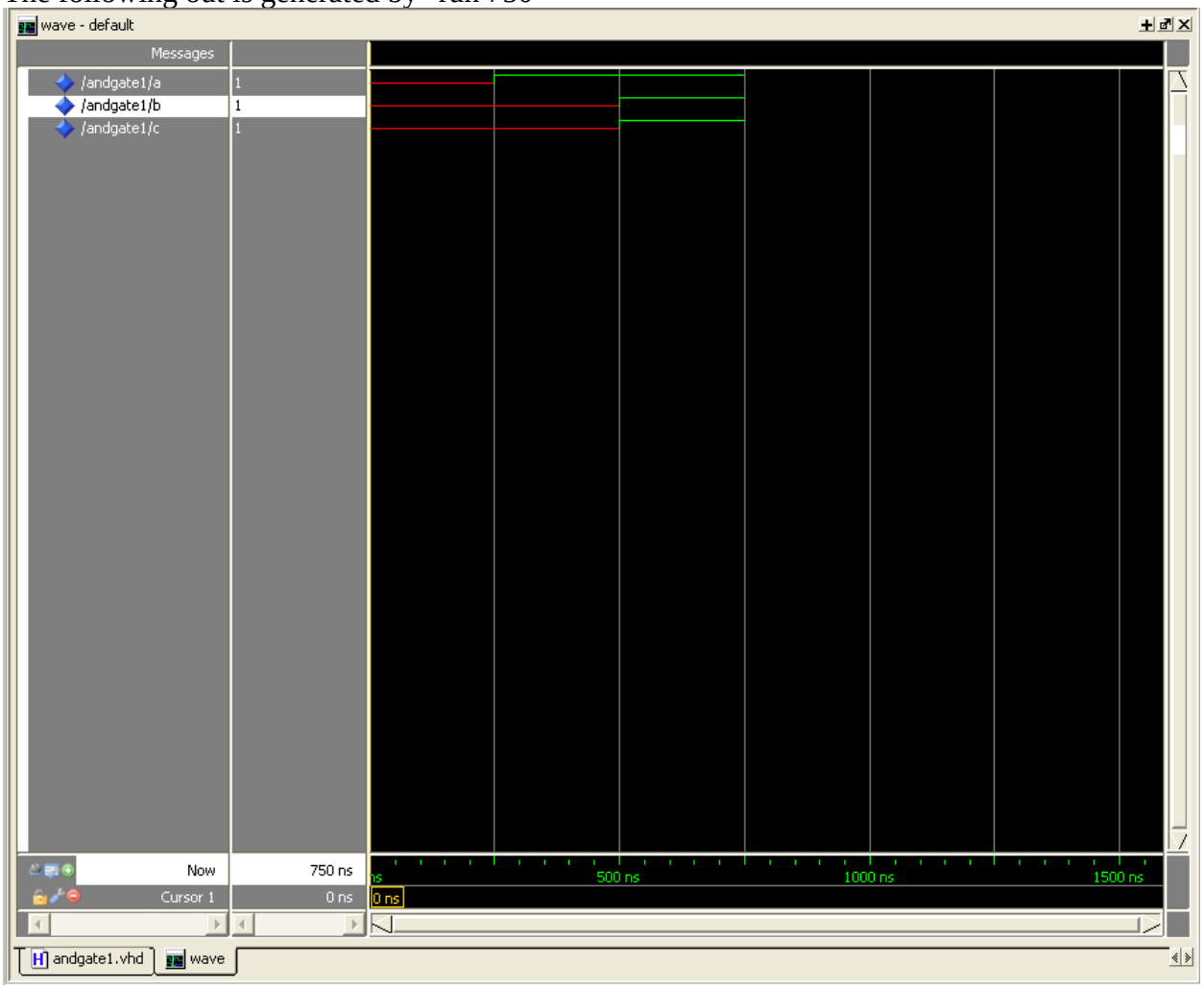
In the ModelSim window, it shows what the command line execution would be
The same thing as above could have been done with signal a by typing "force -freeze sim:/and_gate/a 1 250"

Now type "run 750" in the ModelSim window, which will run the
This will run the sytem for
750ps


ModelSim XE III/Starter 6.3c - Custom Xilinx Version
File Edit View Compile Simulate Add Transcript Tools Layout Window Help
Help
Layout Simulate
0 ns
Workspace
Instance Design unit Design unit type
andgate1 andgate1(s... Architecture
line__14 andgate1(s... Process
std_logic_unsigned std_logic_un.. Package
std_logic_arith std_logic_ar... Package
std_logic_1164 std_logic_1... Package
standard standard Package
Project Library sim Files Memc
Objects
Name Value
a 1
b 1
c 1
wave - default
Messages
/andgate1/a 1
/andgate1/b 1
/andgate1/c 1
Now 750 ns
Cursor 1 0 ns
andgate1.vhd wave
Transcript
force -freeze sim:/andgate1/b 1 500
VSIM 8> run 750

Analyzing Output

The following out is generated by "run 750"



As can be seen, signal a freezes at 1 after a delay of 250ps
Signal b freezes at 1 after 500ps
The red line signifies that the data is unknown, which is try since the data is unknown before 250ps and 500ps
Output c is determing function of the two signals throughout the execution, which ends at 750ps